



ALLO-02-004

September 12, 2003

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/602,228 06/24/03

Ki-Tai Park et al.

HIGH EFFICIENCY TRIPLE WELL
CHARGE PUMP CIRCUIT

Grp. Art Unit: 2828

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on September 11, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 9/19/03

U.S. Patent 6,418,040 to Meng, "Bi-Directional Architecture for a High-Voltage Cross-Coupled Charge Pump," is directed to a cross coupled charge pump that can provide a high positive or negative or negative output voltage depending upon which state the two input voltages of the charge pump are used.

U.S. Patent 6,212,107 to Tsukada, "Charge Pump Circuit and a Step-Up Circuit Provided with Same," discusses a charge pump directed to providing a stepped voltage and includes a leakage current suppression circuit.

U.S. Patent 6,130,574 to Bloch et al., "Circuit Configuration for Producing Negative Voltages, Charge Pump Having at Least Two Circuit Configurations and Method of Operating a Charge Pump," is directed to providing a negative voltage charge pump, wherein each stage contains three of four MOS transistors and has two clocks operating at different phases.

U.S. Patent 6,046,625 to Menichelli, "High Current CMOS Charge, Particularly for Flash EEPROM Memories," is directed to providing a charge pump circuit having multiple mirrored stages that are controlled by logic circuitry that receives a clock signal and an enable signal.

U.S. Patent 5,925,905 to Hanneberg et al., "MOS Circuit Configuration for Switching High Voltages on a Semiconductor Chip," discloses a MOS circuit configuration directed to a high voltage charge pump without using deep insulating wells.

U.S. Patent 5,815,026 to Santin et al., "High Efficiency, High Voltage, Low Current Charge Pump," discloses a charge pump circuit directed to providing a high voltage low current at a high efficiency.

A conventional charge pump circuit based on a diode structure is discussed in "On-Chip High-Voltage Generation in MNOS Integrated Circuits Using Improved Voltage Multiplier Technique," IEEE Journal of Solid-State Circuits, Vol. 11, No. 3, June 1976, pp. 374-378.

A representative charge pump circuit of prior art using a four-phase clock scheme which is described in "A 5-V-Only 0.6um Flash EEPROM with Row Decoder Scheme in Triple-Well Structure," IEEE Journal of Solid State Circuits, Vol. 27, No. 11, November 1992, pp. 1540-1545.

U.S. Patent 5,986,947 to Choi et al., "Charge Pump Circuits Having Floating Wells," describes a pump circuit using a floating well.

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Charge pump circuits using a triple well P-N junction and MOS diodes are disclosed in the following U.S. Patent and publication:

- 1) U.S. Patent 6,100,557 to Hing et al., "Triple Well Charge Pump."
- 2) "A 3.3V-Only 16 Mb DINOR Flash Memory," IEEE International Solid State Circuits Conference, Digest of Technical Papers, 1995, pp. 122-123.

Sincerely,

A handwritten signature in black ink, appearing to be 'SBA', with a long horizontal flourish extending to the right.

Stephen B. Ackerman,
Reg. No. 37761

**INFORMATION DISCLOSURE CITATION
IN AN APPLICATION**

SEP 22 2003
(Use several sheets if necessary)

Docket Number (Optional)

HALO-02-004

Application Number

10/602,228

Applicant

Ki-Tae Park et al.

Filing Date

06/24/03

Group Art Unit

2828

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILED DATE IF APPROPRIATE
	6418040	7/9/02	Meng	363	60	4/9/01
	6212107	4/3/01	Tsukada	365	189.09	12/14/99
	6130574	10/10/00	Bloch et al.	327	536	7/26/99
	6046625	4/4/00	Menichelli	327	536	12/18/97
	5925905	7/20/99	Hanneberg et al.	257	299	7/24/97
	5815026	9/29/98	Santin et al.	327	536	7/19/96
	5986947	11/16/99	Choi et al.	365	189.11	4/9/98
	6100557	8/8/00	Hung et al.	257	299	10/10/96

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
					YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Portmanteau Pages, Etc.)

-	"A 5-V-Only 0.6 μ m Flash EEPROM with Row Decoder Scheme in Triple-Well Structure", IEEE Journal of Solid State Circuits, Vol. 27, No. 11, Nov. 1992, pp. 1540-1545.
-	"On-Chip High-Voltage Generation in MNOS Integrated Circuits Using Improved Voltage Multiplier Technique, IEEE Journal of Solid-State Circuits, Vol. 11, No. 3, June 1976, pp. 374-378.
EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant

Form PTO-1449

INFORMATION DISCLOSURE CITATION
IN AN APPLICATION SEP 22 2003

(Use several sheets if necessary)

Doc No: Number (Opinion)

HALO-02-004

Agenda Item Number

10/602,228

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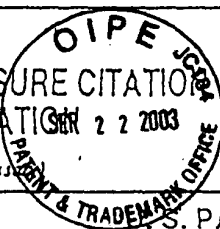
Ki-Tae Park et al.

Filing Date

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Group Art Unit

2828



S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Portion, Pages, Etc.)

"A 3.3V-Only 16 Mb DINOR Flash Memory," IEEE International Solid State Circuits Conference, Digest of Technical Papers, 1995, pp. 122-123.

EXAMEN

DATE CONSIDERED

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